Introduction to Class-D audio amplifiers

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3 Summary
1. Introduction

1.1 Requirements
1.1 Requirements - Power

- Transducer efficiency is low (< 3%)
- High electrical power levels required

<table>
<thead>
<tr>
<th>Typical sound</th>
<th>$P_{\text{acoustic}}$</th>
<th>$P_{\text{electric}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Refrigerator (background noise)</td>
<td>0.1 uW</td>
<td>3.3 uW</td>
</tr>
<tr>
<td>Talking (moderate music level)</td>
<td>10 uW</td>
<td>0.3 mW</td>
</tr>
<tr>
<td>Playing kids (typical listening level)</td>
<td>10 mW</td>
<td>33 mW</td>
</tr>
<tr>
<td>Trumpet (high listening level)</td>
<td>0.3 W</td>
<td>10 W</td>
</tr>
<tr>
<td>Concert (very high listening level at long distance)</td>
<td>100 W</td>
<td>3.3 kW</td>
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[1]
1.1 Requirements - Performance

- Signal quality needs to be high since the human ear is the most sensible organ in the human body
- Signal to noise ratio (SNR)
  - Consumer and automotive: > 110 dB
  - Professional equipment: very strong dependent on distance from speaker to listener
- Distortion: < 0.01 %
- Frequency range: 20 Hz to 20 kHz
  - Note that the eye can not follow 100 Hz at the TV!
1. Introduction

1.2 Block Diagram
Intro
Realization
Chosen Problems
Summary

1.2 Block Diagram

- Low Freq. Feedback
- High Freq. Feedback
- Error Amplifier
- Modulator
- Power Stage
- Low Pass Filter
2. Realization

2.1 Error Amplifier

2.1.1 Digital
Digital control usually intrinsically contains the modulator

Power stage requires a single bit stream

=> sequential coding

SNR and highest audio frequency determine the speed of the microcontroller or digital signal processor (DSP)
2.1.1 Error Amplifier – digital - timesteps

Quantization interval: $\Delta t = t_1 - t_0$
- $T_{\text{bit-stream}}$: period of switching frequency
- $T_{\text{audio}}$: period of highest audio frequency

Sampling theorem: $T_{\text{bit-stream}} \leq \frac{T_{\text{audio}}}{2}$
2.1.1 Error Amplifier – digital – DSP speed

- SNR should be 110 dB
  - => Bit depth
  \[ N = \log_2 \left( 10^{110/20} \right) = 18.3 \text{ bit} \]

- => One quantization interval:
  \[ \Delta t = \frac{1}{2^{19} \cdot 20 \text{ kHz}} \approx 95.4 \text{ ps} \]

- => DSP output frequency:
  \[ f_{DSP} = \frac{1}{\Delta t} \approx 10.5 \text{ GHz} \]

- Not achievable with DSPs known in the art
- Solutions: PEDEC [2], [3] and noise shaping
Noise shaping transfers noise from one frequency band into another one.

![Graph showing magnitude of NTF with different orders and phase characteristics.]
2. Realization
   2.1 Error Amplifier
       2.1.2 Analog
2.1.2 Error Amplifier – analog

Analog error amplifiers usually are operational amplifiers (OPAMP)

- SNR of the system is determined by the noise floor of the OPAMP
- Distortion of the system is mainly determined by the linearity of the OPAMP
Simple case: PI controller

For stability reasons zeros are required

Those might require further poles for compensation

\[ H(s) = \frac{R_2}{R_1} + \frac{1}{sR_1C} \]
2.1.2 Error Amplifier – analog – noise

- For 30 V output voltage:
  - 225 W into 4 Ohm load
  - Gain from error amplifier to output stage:
    - 60 V supply @ power stage (= $V_{rail}$),
    - 5 V supply @ error amplifier

$$N_{out} = \frac{S_{out}}{10^{\frac{110}{20}}} \approx 95 \mu V$$

- Gain from error amplifier to output stage:
  - 60 V supply @ power stage (= $V_{rail}$),
  - 5 V supply @ error amplifier

$$G = \frac{V_{supply\_power\_stage}}{V_{supply\_error\_amplifier}} = 12$$

- Error amplifier noise:

$$N_{ea} = \frac{S_{out}}{G} \approx 8 \mu V$$

- Most critical is the noise level in the frequency range from 1 .. 4 kHz
2. Realization
  2.2 Modulator
    2.2.1 Self Oscillating
2.2.1 Modulator – self oscillating – block diagram

- **Phase shift controlled oscillating modulator**

- **Hysteretic controlled oscillating modulator**
2.2.1 Modulator – self oscillating - properties

- Varying switching frequency in dependency of input level
- Conditionally stable intrinsically
  - => no stability problems
- High gain-bandwidth product
- Hysteretic varies frequency wider than phase shifted
- Other variants:
  - natural self oscillating modulator
  - Delay controlled oscillating modulator
- Higher EMC
- Less controllable EMC
2. Realization
   2.2 Modulator
      2.2.2 Sigma Delta
2.2.2 Modulator – sigma delta – block diagram

As known from digital to analog converters (DACs) and analog to digital converters (ADCs)
Inphase, quadrature and interleave
2.2.2 Modulator – sigma delta – spectrum

- Interleaved frequency contents
2.2.2 Modulator – Sigma-Delta – Pros and Cons

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<td>✓ High out-of-band noise levels (EMC)</td>
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Pros:
- Simple feedback
- Preferred for digital inputs
- Simple noise shaping possibilities
- Interleave possible

Cons:
- High out-of-band noise levels (EMC)
- Clock generator required
2. Realization

2.2 Modulator

2.2.3 Fixed Frequency
Output of clock generator (carrier / reference) can either be a sawtooth or a triangle waveform.

This determines about single edge modulation or double edge modulation.

Multiple carriers can generate interleave.

Further overview: [7]
2.2.3 Modulator – fixed frequency (PWM) – signals

Inphase, quadrature and interleave N=2
2.2.3 Modulator – fixed frequency (PWM) – signals

- Inphase, quadrature and interleave N=4
2.2.3 Modulator – fixed frequency (PWM) – spectrum

Intro
Realization
Summary

Interleave N=2
2.2.3 Modulator – fixed frequency (PWM) – spectrum

Interleave N=4

Intro
Realization
Summary
2.2.3 Modulator – fixed frequency (PWM) – properties

- Fixed frequency modulators need an external clock generator
- PWM has higher predictable EMC
- Interleave is possible
- Further information about interleave can be found in [8]
2. Realization

2.3 Power Stage
2.3 Power Stage – block diagram

- Increases signal level
- MOSFETs: n/n or p-/n-channel versions
- Power supplies need to be chosen carefully
2. Realization

2.3 Power

2.3.1 Half Bridge
2.3 Power Stage – half bridge

Intro
Realization
Summary

- Power supply pumping
- No interleave possible
- Limited output power
- Requires balanced power supply
- Less board or chip area required
2. Realization

2.3 Power

2.3.2 Full Bridge
2.3 Power Stage – full bridge

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- No power supply pumping
- Interleave possible (even higher than 2)
- Theoretical unlimited output power
- Can be supplied with single supply
- More board or chip area required
2. Realization

2.4 Filter
2.4 Filter - overview

Intro

Realization

Summary

Filter suppresses energy in EMC interested frequency ranges

Filter passes audio unchanged

=> Low Pass

Filter is applied to the amplified bit-stream

=> High energy levels are driven through the filter
The energy levels driven through the filter usually never allow an active filter and none of those is known in the art.

The filter is required to be lossless to keep the advantages of the efficiency common to all Class-D amplifiers, therefore consisting only of reactive components.

The cut-off frequency of the filter needs to be between the highest audio frequency and the lowest switching frequency, to allow undamped passing of the audio signal and provide suppression of the high frequency material.
The lower the cut off frequency should be, the bigger the capacitors and inductors in the filter are. Big values in those places cause increased parasitics within those, which have negative impact on the overall performance of the filter.

The higher the frequency rises, the more also the traces on a board take effect.

Undamped filters cause an overshoot in the spectral output of the amplifier while damping introduces losses.

The materials used in the filter components – especially the cores of the inductors, as those are getting magnetized – need to be carefully chosen together with the used switches and the switching frequency (or switching frequency range) as a trade off between static and dynamic losses. Both of those loss mechanisms can be seen in all components which are applied to high voltage or high current stress. A more detailed reflection on those choices can be found in [9]
Typical cutoff frequency: 50 kHz

Typical switching frequencies: 200 kHz .. 500 kHz

Typical values:

- L: 10 uH .. 40 uH
- C₁: 100 uF .. 500 uF
- C₂: multiple hundred nF
- C₃: multiple hundred nF
- R: multiple Ohms
2. Realization

2.5 Feedback
2.5 Feedback – error sources

- Delay times in comparator, level shifter, gate drive and switches,
- Finite rise and fall times of the signal edges due to finite gain-bandwidth products in components,
- Nonlinearities in all of the above components and the output filter,
- Power supply perturbations,
- Varying component characteristics with temperature and humidity as well as varying operation points (due to the large signal nature of an amplifier)
2. Realization

2.5 Feedback

2.5.1 High Frequency Feedback
2.5.1 Feedback – *high frequency feedback*

**Intro**

**Realization**

- High frequency feedback is taken from amplified bit-stream
- Modulators are multiplying signals
  - $\Rightarrow$ frequencies can be added and subtracted
  - $\Rightarrow$ subtracted frequencies can be mixed down from high frequency band into audio band
- $\Rightarrow$ need suppression

**Summary**
Loops not closed, but high frequency fed into input => aliasing distortion!
3 kHz component causes 0.108% third harmonic distortion
2. Realization

2.5 Feedback

2.5.1 Low Frequency Feedback
Low frequency feedback is taken from behind the filter

- 180 ° phase shift involved
- Impacts stability
2.5.1 Feedback – high frequency feedback – closed loops model

2.5.1 Feedback – high frequency feedback -

- 22.2 dB suppression at 3 kHz
- => 0.008 % third harmonic distortion
3. Summary

Switch mode amplifier design involves a lot of engineering disciplinaries:
- circuitry
- power electronics
- active and passive components
- high frequency circuit design
- EMC
- control theory
- information theory
- signal theory and waveform analysis
- measurement technology
- digital technology
- programming
- Microelectronics

As well as: mechanics, acoustics, physics, biology, project management, economics and a LOTS OF FUN!


Thank you for your interest!

I am looking forward to your questions!